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Biography of a Brat

This is an account of the exploits of three fifth year pupils from Blessed Edward Oldcorne School, Worcester, and their 1980 School Design Prize winning entry, the BRAT. BRAT is an acronym for Bell Ringing Automatic Timer, although, when the project was started no specific name was in mind.

BRAT, another example of necessity being the mother of invention, is the brain child of Nicholas Ash, Adrian Trace and Michael Holloway, and is an electronic system for ringing the school bells, at prescribed times, automatically. Prior to the installation of BRAT the school bells were rung manually by a senior pupil with an accurate wrist watch. Although this system was adequate, within limits, there was a time factor involved, 42 minutes per day, in ringing the bells manually. This represented some 10½% of each school day being lost to the pupil and over an academic year this amounted to 3.8 weeks lost.

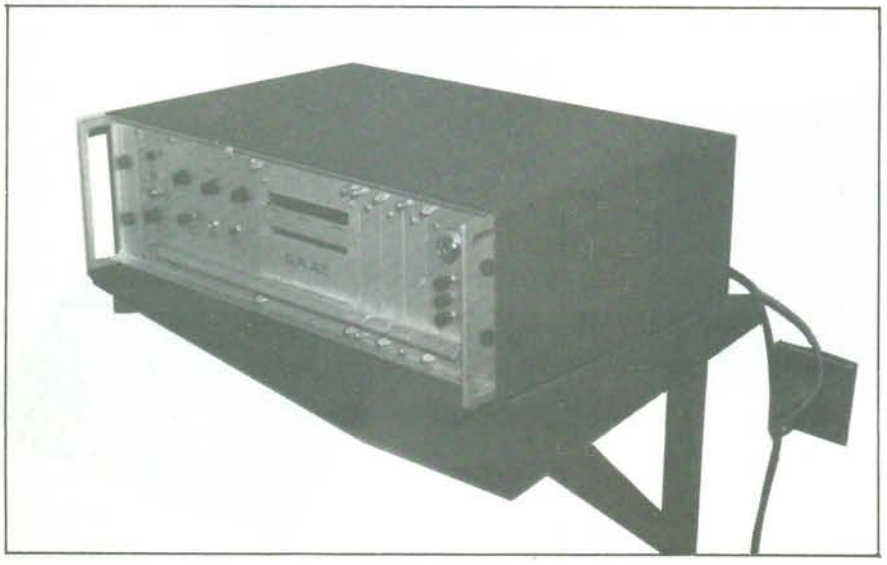
Nicholas Ash was the one responsible for bell ringing and feeling that he was missing valuable lesson time he set out to find a suitable alternative persuading Adrian and Michael to join him in his quest.

Electronics, as yet, has not figured strongly in the Science curriculum of the School, and although the Physics teacher spent some considerable time discussing the project with the boys, they had to seek outside help to supplement their own knowledge and experience. Nicholas' father works in the electronics field and proved to be a suitable devils advocate for their design.

As with all design work the boys examined several avenues capable of satisfying their design brief before finally selecting BRAT. By a process of elimination four final designs were considered –

1. Remote Control Device.
2. Sangamo Clock System.
3. A Punched Tape System.
4. An Electronic, fully automatic, System.

The completed unit



The remote control device involved a transmitter, which was to be kept with the bell monitor, and a receiver, linked to the existing bell push in the Secretary's Office. Although the system had some merit it was discarded because the punctuality was still dependent upon the memory of the bell ringer. Further minus points to this sytem was the need for a radio transmitting licence, renewable every five years, and the distinct possibility of radio signal absorption by the excess of metal in the school structure.

Any system that could be designed incorporating a Sangamo Clock, already available on the market, would have some merit. However, yet again it was discarded because of the inprecise nature of setting the clock. The lesson times to be considered were multiples of 35 minutes and the setting accuracy of the Sangamo was $\pm$ 5 minutes.

Punched tape systems have been in operation in industry for controlling machine tools for some time, as they have for early memory storage and recall systems. They involve motors which drive tapes with holes punched in. These holes, when passing over a pair of contacts would cause the contacts to close together forcing a relay to activate the bells. The system considered required a constant speed motor, which was available and through suitable gearing a close approximation of school time was achieved. However, due to extremely lengthy tape, the possibility of damage and wear, and the difficulty of producing the required accuracy when punching the holes, this system was also rejected.

From these ideas it was finally decided that a system, which was stationary in the Secretary's Office, accurate and punctual was necessary. Fourteen bells were needed to be rung each day, plus the extras when wet weather needed to be signalled and these conditions prescribed two variations of an electronic system.

1. A handwired logic device.
2. A micro processor software device.

Choice two was discarded on the grounds that for a one-off device, it would have been too expensive, since the cost of programming micro-processor is about £100 per day.

This left the handwired logic device which was to become the BRAT.

The design finally settled upon consists of the following:–

(a) A proprietory enclosing sheet metal case with a withdrawable standard 19″ sub-chassis.

(b) Plug-in cards, each with a protective front plate and retaining screws, having a handle for ease of insertion and withdrawal. Each plug-in card had printed circuit board(s) on which are mounted solid state 'chips'.

The board numbers are defined as follows:–

Board 1 – Oscillator and decoding for week clock.

Board 2 – Decoding of pre-set bell-ringing times.

Board 3 – Operation of relay.

Board 4 – Output from Board 1 conversion into a digital readout.

Display Module – Containing a display with seven-segment-displays for Hours, Minutes and Seconds, together with a display reading which day it was indicating.

Odds Board – Containing circuitary for updating and the Supplies Healthy network.

(c) Commercially available power supplies are used to give the necessary operating voltages.

The electrical circuitary is generally as follows:–

1. The 240 volt supply is filtered to prevent spurious or transient interference, and feeds three 240 to 5 volt 1 amp power modules, each separately fused. One supply is used to give the 5 volt logic level, one is used to give the Lamp Supplies at 5 volts and is also connected in series with the third 5 volt supply moule to give a 10 volt supply for the CMOS circuitary and external relay.
2. A crystal control oscillator operates at 4.194304 MHz. This is divided down by a CMOS 2^{24} counter. Dividing by 2^{21} gives half second pulses and by 2^{22} gives one second pulses. The two outputs are fed through CMOS to TTL drivers.
3. The half second pulses are fed to a monostable multivibrator giving 1 ms. pulses after a delay of ten microseconds after the rising edge of each pulse.
4. The one second pulses are fed to decade counters which are programmed to give divide by six, seven, ten or twenty-four. In this way the BCD outputs of the counters are arranged to give a 24 hour/week clock with Days, Hours, Minutes, and Seconds outputs.
5. The decade counter outputs are fed to temporary latches which are clocked every second when the data is stationary.
6. The temporary latch outputs are fed to BCD to seven segment decoders to give a visible readout.
7. The latch outputs are also fed to eight input NAND gates looking at hours and minutes so that an output can be given at a pre-programmed time.
8. By use of NOT gates and two input AND gates some of the eight input NAND gates are used to perform two switching functions.
9. The programmed output are arranged to operate a relay for a pre-set period of time which is adjustable by means of a potentiometer controlling the time interval of a monostable multivibrator.
10. Setting push button switches are provided to allow the Days, Hours and Minutes to be advanced at second intervals.
11. The power supplies are monitored into a 'supplies healthy' circuit which is indicated by means of a L.E.D.
12. A manual over-ride is provided to enable bell ringing at non-programmed times.
13. A security key allows the setting switches to be disabled to prevent unauthorised operation.

Board 1 was made to accommodate the week clock, whereby the outputs of the times could be sent to both the display board (Board 4) and the decoding board (Board 2).

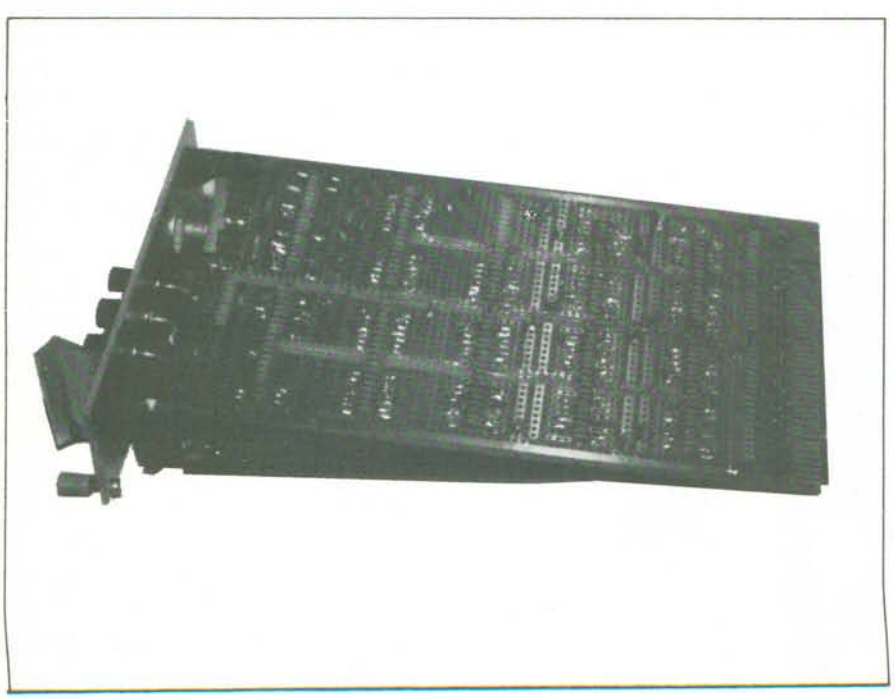
Two possible methods for the timing were considered:–

1. A clock module.
2. A second decoding clock.

The clock module was decided against as there was no foreseeable means of decoding the times into Board 2, so as to generate the bell-ringing times.

A second pulse clock was therefore decided upon, involving the generation of the one second pulses.

Right: Board 1 Component side
Below: Board 1 Wiring side



There were two choices:—

1. Dividing the mains supply by fifty.
2. Using a crystal controlled clock.

Using the mains supply to generate the one second pulses was decided against because of the fluctuations in the mains supply which would adversely affect the clock display. They therefore decided to use a crystal controlled clock. They found a 4.194304 MHz crystal which divided by 2^{22} would give 1 Hz. This presented a problem as they could not find a TTL chip which divided by 2^{22}, in fact the greatest was 2^{16}. After some research they came across a CMOS chip which operated up to a 2^{24}, they, therefore, decided to use this chip, unfortunately it needed a higher voltage level i.e. 10 Volts, and this is the reason for the extra power supply module.

On the CMOS chip 4521 it was essential that this does not come into contact with any static electricity and involved careful work when inserting this chip into its socket.

Sockets were decided on this board for ease of maintenance and withdrawal of dud chips.

The outputs of CMOS chip are equivalent to 2^{21} and 2^{22} dividing of the osillator. This gives half and one second pulses respectively.

These pulses are sent to a CMOS to TTL chip (75270) since these two chips operate at different levels. The one second pulses are then sent to a terminal and hence to the lock switch. The half second pulses are then sent to a monostable multivibrator 74121 which is arranged to give a 1 mS pulse after a 10mS delay, that is used as the clocking pulse for the quad bistable latches 7475.

The one second pulses are then sent to the first decade counter at the Ain. input (pin 14). The output A (pin 12) from the decade counter is also fed into the Bin. input (pin 1). Pins 2 and 3 (reset to '0') are not used and therefore must be placed at 0 Volts. Pins 6 and 7 (reset to '9') are linked on all the decade counters except the last one, so as to provide a reset facility. Pin 10 is the 0 Volt supply. Pin 5 is the Vcc supply i.e. + 5 Volts. The outputs A, B, C and D correspond respectively to 2^0, 2^1, 2^2, and 2^3. These outputs are fed to the quad bistable latches (K-Q) which moves the data input on A, B, C and D and gives the outputs on QA, QB, QC and QD when the second clock pulses are brought in on pins 13 and 4. On the 7475 0 Volts is on pin 12, and Vcc on pin 5. The outputs of the latch are then fed to terminals.

On the second decade counter the Ain. input becomes the D output of the previous 7490. By using the C and B outputs corresponding to 4 and 2 and the reset to zero facility it is possible to reset the decade counter to '0' when '6' is normally represented.

All other decade counters work on the same principle. All inputs to the latch which are not used are tied to Ov to prevent spurious operations. The outputs of the highest binary digit and the Ain. input are between seconds, hours and days are also fed to terminals to provide an update facility.

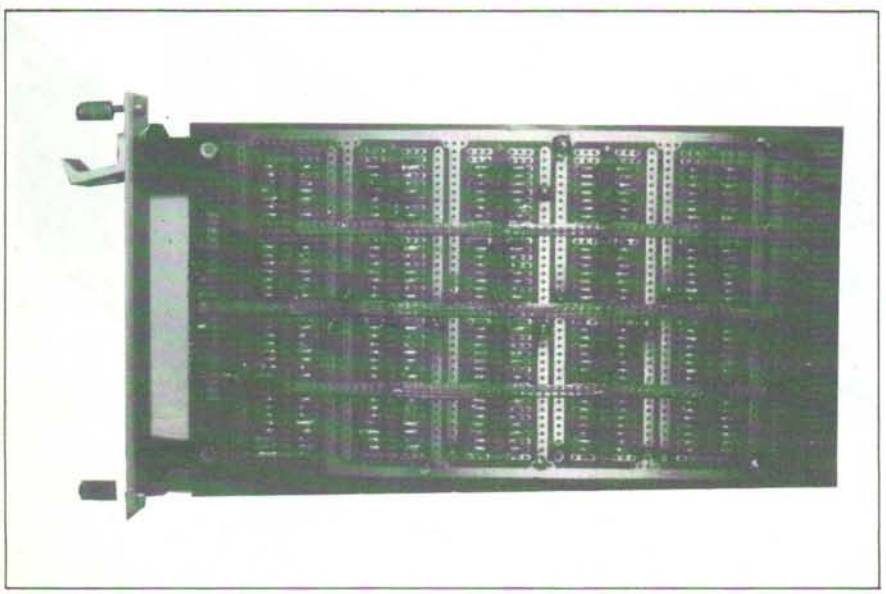
On the last 7490 the divide by seven network, instead of resetting to '0' when '6' should be represented it is reset to '9' thereby giving seven different outputs. After the values A, B, C and D have passed through the quad bistable latch they are then passed into a B.C.D. to Decimal chip (7442(r)), the values 0,1,2,3,4,5 and 9 are then sent to terinals, '0' representing Sunday and '9' representing Saturday.

The section of the system which was housed on Board 2 was that of decoding the clock pulses and producing a pulse at the correct time which would activate a relay.

The requirement stipulated that the bell should only ring during school time: e.g. Monday to Friday, so that the system had to include a day enable.

In addition because the times required in the morning did not coincide with those in the afternoon, using the twelve hour clock, it was decided to have a twenty-four hour clock to prevent the bells ringing at night, rather than a twelve hour clock and a p.m. and a.m. indicator.

Board 2
Wiring side



Final Design

The final design utilised digital techniques using TTL logic gates. This was done using 8 input NAND gates, Hex. inverting Schmitt triggers and 2 input AND gates.

The time enters the board via pins 4-15 and is split up into hours consisting of tens and units, and the units being made up of 2^0, 2^1, 2^2, 2^3, and Mins. which consist of tens in the form of 2^0, 2^1, 2^2, and units in the form of 2^0, 2^1, 2^2, 2^3. Therefore before any final design could be worked out, the required times had to be translated into a code.

The HEX inverting Schmitt triggers are used to prevent the output of the gate going low at any other time than that which is required e.g. without

the inverting gate connected to tens of hours prevents bell triggering at 18.49. The two input AND gates are used when the number of connections inverted or otherwise is greater than the number of inputs of the NAND gate.

Modules were decided for this board to assist in the replacement of dud chips.

Board 3 deals with the operation of the relay from the time codes from Board 2 and has the circuitary to eliminate bell-ringing operations on Saturdays and Sundays.

Each of the eleven outputs from Board 2 enter 8 input NAND gates via pins 16-26. These outputs being normally 1 and during a bell ring code becomes 0. The outputs from the 7430's are therefore normally 0 and become 1 during a bell ring. The outputs are fed through on NOR gate (7402). This is then fed into a monostable multivator which is arranged to give bell ringing duration between 0-7 and 8 secs. This input is normally 1, drops low during the bell code and then rises back up to 1 at the end of the bell code. On this rising edge the monostable multivator is fired (this is the reason for the coding being a minute earlier). The time duration of the bells can be altered by adjusting the potentiometer on this board. The output of the monostable multivator is sent to the A input of a relay driver. This is normally 0 but goes to 1 during the time the bell is rung. A break is provided between the monostable multivator and relay driver pins 13 and 14. This break is taken to the lock switch to prevent bell-rings during the update mode.

The days enter via pins 30-36. These are all passed through a hex schmitt inverter and then through a darlington driver. This is necessary as more than one L.E.D. segment is being lit up. The outputs of the darlington driver are all 1 except the day which is 0. These are then passed to pins 5-11. The input of the days Monday to Friday pins 31-35 are also sent to an 8 input NAND gate. Therefore the output of this gate is 0 on Saturdays and 1 on Mondays to Fridays.

The output is then fed to the B input of the relay driver. The output of the relay driver is 0 only when the bell is to ring at programmed times but not on Saturdays and Sundays. An 0 output at the relay driver allows the relay to become energised. The output is then fed to three terminals each.

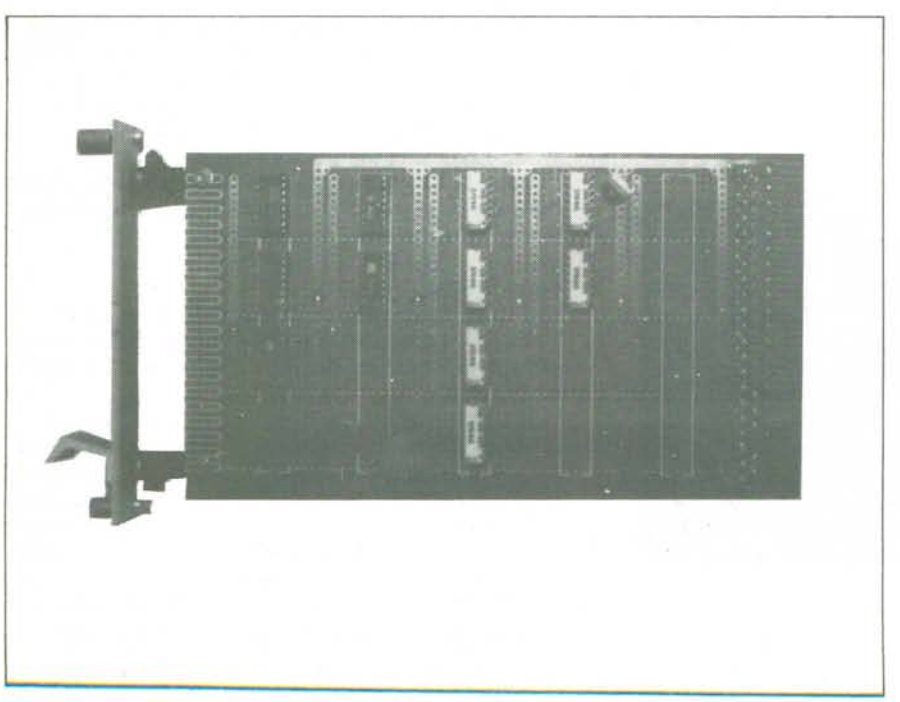
Modules are chosen to assist in replacing dud chips.

The values of QA, QB, QC and QD, the outputs from the quad bistable latches on Board 1 are fed to the inputs A0, A1, A2 and A3 respectively on Board 4. The chip used in the 7447A which converts the B.C.D. outputs into signal levels required to drive a seven segment display. Outputs from the chip are each fed through a 270*n* resistor. Resistor networks, commercially available are used instead of normal resistors. The outputs of the resistors are then fed to board output terminals.

On the 7447A chip, Ov is on pin 8, Vcc at 5 Volts is on pin 16. A ribble blanking facility is built in, i.e. cutting out any unwanted zero's on the left of the display. This is provided on the chip by wiring pin 5 to pin 4 on the succeeding chip. The last chip, on pin 5 is then wired to Ov. A lamp test facility is also provided on the chip. These are wired up in parallel and fed to a terminal, in order to test the lamps this terminal must be sent to Ov.

Because of the excessive number of inputs and outputs, it was necessary to use a P.C.B. which had a double sided edge connector. Terminals on side A and side B.

Right: Display module
Below: Board 4
Component side



The Display Module was designed to give a digital readout of days, hours, minutes and seconds.

The module is made up of three pieces of veroboard mounted with two 'carry-up' rails and a front panel. The front panel occupies, near the top, 8 seven segment red L.E.D. These are spaced as hours (2), spare, minutes (2), spare, seconds (2). These are mounted on sockets for ease of insertion and withdrawal. These are all mounted behind a RED filter on the 5" panel.

The day display took a lot of research. The first idea was to display the day on a seven segment chip, but this caused problems when representing letters like 'M'. There was also the possible idea of lighting a single L.E.D. underneath the word 'Monday'. The final design was decided upon because of its professional look. This consisted of a 30 bargraph-display on top of which we had to fix letter transfers. This again was mounted behind the filter.

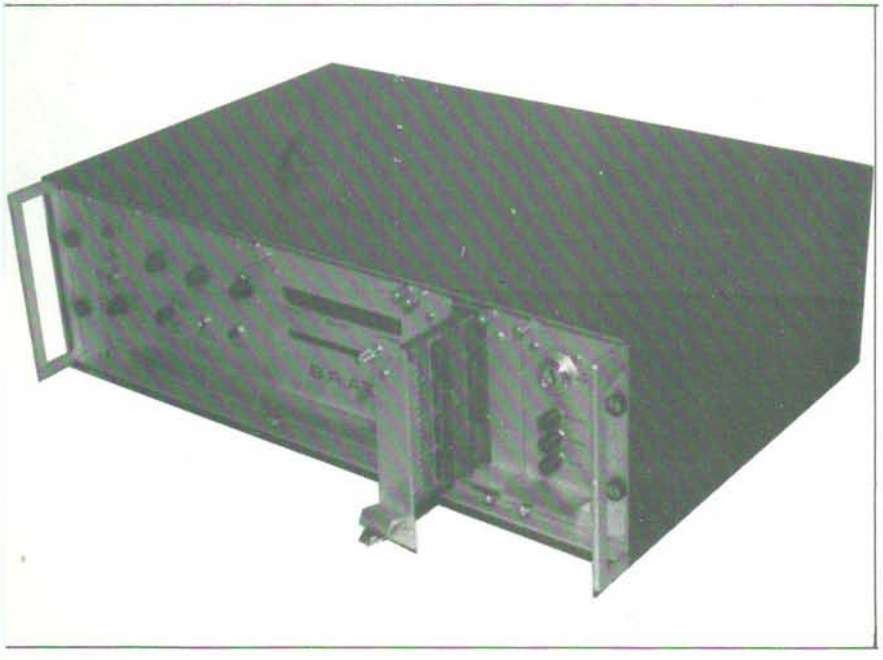
The front cover also holds 4,270*n* register network mounted in modules for use with the day display. The veroboards are held together with brackets, and the front cover is held with bolts to the 5" front panel and therefore can be inserted and withdrawn like any other board.

The wiring is done with a P.V.C. coated 20-way ribbon cable.

The Odds Board contains the circuit for updating and the power supplies healthy network.

The first design for updating consisted of placing one second pulses directly onto the Ain. input of the 7490 and then switching the D output of the previous 7490 back over. This design unfortunately did not work and resulted in the display jumping when the switch was re-set.

Withdrawal of cards.



The design now installed, although not perfect is adequate. This consists of a series of time delay networks by resistors and capacitors to reduce switch bounce. The clocking pulses and the time delay are sent to a two input-schmitt NAND gate. The mins. in and secs; hours in, and secs; days in and seconds are dealt with in a similiar manner. The output of the gates are then inverted to give the outputs clocking pulses, mins out, hours out and days out respectively.

The mains supply comes in on the back panel via a 5A mains filter to protect the power modules from mains fluctuations. A mains ON/OFF switch is then provided. A neon indicator shows whether the power is 'on' or 'off'. All the mains input is brought to a terminal block in grey cable. The outputs of the three power modules is then taken from the power module terminal blocks in black mains cable to a terminal block. The outputs are then taken to the fuses and supplies healthy network out to the following:

P.S.U.1 – T.T.L. Logic 1.5A fuse
P.S.U.2 – + 5v Display 1.5A fuse
P.S.U.3 – + 10v Logic 0.5A fuse

A mains fuse rated at 5A is also provided for safety.

The terminal block is located on top of power supply units 1 and 2, to the left of the sub-assembly. Power Supply Unit 3 is between the display module.

The casing of the system is all earthed via the supply modules.

The supplies healthy network works via two D.I.L. reed relays. If the outputs of P.S.U.1 and 2 are on, the relays are energised. If unit 3 is on, this supplies the Vcc supply to the L.E.D. If the relays are both energised, the other side of the L.E.D. is taken to Ov, therefore, switching the green L.E.D. on. The diodes of P.S.U.1 and 2 are to prevent feedback on this circuit.

The system was built up within a standard nineteen inch sub-rack system. Each printed circuit board has a 1" panel front and are mounted on card rails for ease of assembly, etc. Board 1A and 1B are on a 2" panel with the keyswitch and update switches. The board cards and display module have knurled nuts for ease of insertion and withdrawal. The fuses panel contains the fuses to Power Supplies 1, 2 and 3 rated at 1.5A, 1.5A and 0.5A respectively. This also contains the manual bell ring switch, a L.E.D. indicating bell rings when the lock switch is in the update mode; and a 'Press to Hold' switch. This is all mounted on a 5" panel. To the left of this panel is the mains panel, a 2" panel. This contains the On/Off toggle switch, the neon indicator (displaying the mains input), the 'supplies healthy' green L.E.D. and the mains fuse (5A). This panel does not have a handle as it would be dangerous to remove it. Both this panel and the fuses panel have screw fastenings instead of knurled nuts as a safety aspect.

The mains supply is kept well away from the T.T.L. logic. The power supplies are also kept away

as they generate heat. The system uses a 0.5" tapping rack system. This is all enclosed in a proprietary sheet steel case. The back of this case is removeable by unscrewing the six posidrive screws. The front screws (two on each side) can also be removed so that the whole sub-assembly can then be removed by sliding the assembly forward and feeding the back panel through the case.

As may be gathered from the foregoing the project entailed a considerable amount of work and time. The time scale spans from September, 1979 to installation in February, 1980.

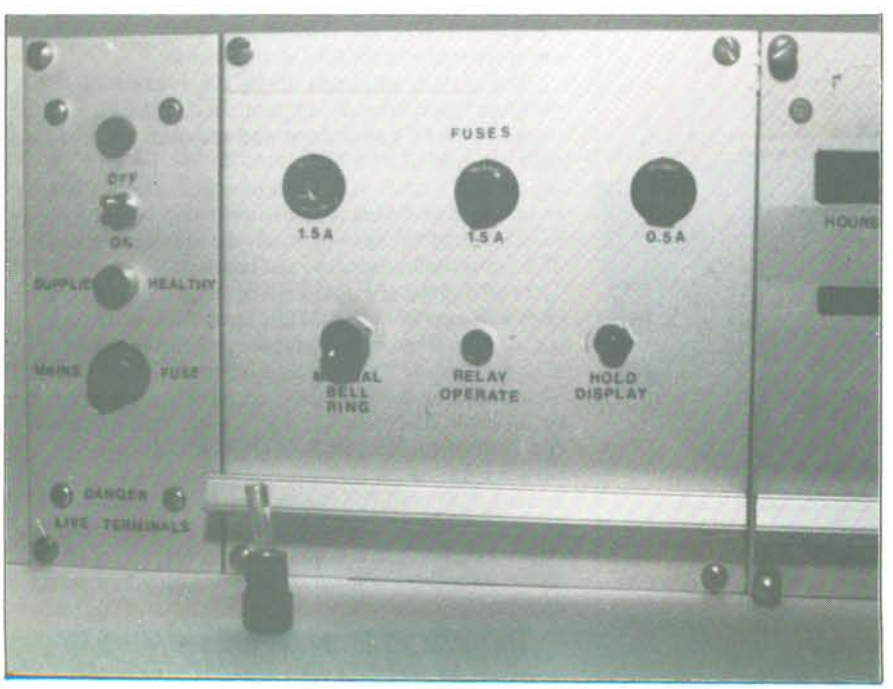
The installation created some minor problems relating to the power supply in the School, consequently when the initial connections were made fuses blew and, in exasperation, the equipmen came in for some school boy invective hence BRAT or so they tell me!!

The total length of time from initial design consideration to the installation and testing was comparatively short and the boys were heavily engaged in academic study at the time thus leaving only evenings and weekends for the project.

As a further indication of their tenacity, these pupils, along with many others in the School were deprived of the facilities of the Art/Craft complex with which they were familiar due to its complete destruction by fire, needless to say their examination course work was also lost, this having to be re-done in temporary workshops.

As a direct result of their enterprise the school now has an up to date and reliable system with which to regulate the day and their prize was certainly earned.

Below: Designers (from left Michael, Nicholas and Adrian)
Bottom: Mains and fuses panel



Below: Update panel